KALGAONKAR PARTH SAMEER

Course : **B.E. (Hons.)**, Electrical & Electronics, 2020
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CGPA : 7.39

ACADEMIC DETAILS

COURSE	INSTITUTE/COLLEGE	BOARD/UNIVERSITY	SCORE	YEAR
CLASS XII	Hislop Junior College Nagpur	Maharashtra State Board of Secondary and Higher Secondary Education	87.23 %	2016
CLASS X	Kendriya Vidyalaya Vayusena Nagar Nagpur	CBSE	95.8 %	2014

Subjects / Electives	Digital Signal Processing, Embedded System Design, Digital Design, Microprocessor Programming and Interfacing, Operating Systems, Device Drivers, Computer Architecture
Technical Proficiency	X86 Assembly, FPGA prototyping, RTL Design, Embedded Systems, Hardware Description Language, Verilog, C Programming

SUMMER INTERNSHIP / WORK EXPERIENCE

Student Trainee, Samsung Research Institute Bangalore — **May 2019 - Jul 2019**

- Worked on adding features to existing IoT platform.
- Integration of feature with existing samsung ecosystem and framework.
- Gained experience of working in a team in a corporate environment.

Project Trainee, Efftronics Systems Pvt Ltd. — **May 2018 - Jul 2018**

Worked in multiple projects including:

- A data acquisition unit for a flow meter in smart water applications.
- Implementation of Wi-Fi communication using XigBee Wi-Fi RF module for an indoor air quality monitoring system to communicate with central TCP server over internet as well as in local network.
- Data analysis for real time location system to find out the optimum location of hotspot to cover complete office flow.

PROJECTS

User-Space Library for LED panels - Device Drivers — **Jan 2019 - May 2019**

- Created linux device driver for LED panels based on HUB12 protocol.
- Userspace text rendering using FreeType library.
- Scalable to create daisy chains of multiple panels for large displays.

Design and Implementation of SPI memory controller on FPGA using Zynq SOC - Interfacing of peripherals in embedded system

Jul 2018 - Present

- To gain practical experience in communication on SOCs through AXI and SPI interface for student nanosatellite.
- Implemented on the Xilinx Zedboard on board a student nanosatellite for hyperspectral imagery. I am trying to interface the FPGA to SPI memory so that the image data can be transferred onto the FPGA for compression and subsequent transmission to the ground station.
- I am working under the guidance of Dr. Chandra Shekhar (Sr. Professor Emeritus, Department of Electrical and electronics engineering).

Calibration Testing of Flow meter Data Acquisition Unit - Embedded Systems — **May 2018 - Jul 2018**

- Undertook the calibration of an ultrasound based flow meter data acquisition unit.
- Work involved collection of samples in various and checking instrument accuracy for various configurations of the on board Time to digital converter and the analog front end.

Implementation of CCSDS Hyperspectral Image compression algorithm on FPGA - FPGA prototyping — **Aug 2017 - Present**

- Creation of CCSDS Hyperspectral Image compression IP for use onboard the nanosatellite in Team Anant.
- Work involves RTL synthesis and verification on Zynq-7000 SoC.
- All system Architecture decisions are made by the team itself.
- Current work involves the synthesis of the image datapath and the control.
- Work also involves design of payload camer image dataflow to maximise throughput. Camera is interfaced to the SoC using USB 3.0

POSITION OF RESPONSIBILITY

System Engineer - Team Anant, BITS Pilani — **Apr 2019 - Present**

- Team Anant is a group of passionate with an objective to design, build, and launch a 3U nano-satellite with a hyper-spectral camera as payload.
- FPGA is used to implement computationally intensive compression algorithm.
- As system Engineer my role is to ensure smooth functioning between the teams from various subsystems.
- Ensuring technical soundness of all subsystems and integration of the System as a whole.

Vice President, Design - BITS Leadership Summit — **Jan 2018 - Feb 2018**

- BITS Leadership summit (BLS) was a nation wide conference that aimed to inspire the change makers of tomorrow to transform the world into a better place.
- Work involved creation of all visual content for the summit including the summit logo, the social media content, outreach brochures, sponsorship leaflets, publicity material and the like.

Publicity Head - Maharashtra Mandal **Jul 2017 - May 2018**

- Work involved creation and distribution of publicity material for all the events of the cultural association and management of all the social media handles.
- Majority of responsibilities revolved around creation of graphic content for use both in the events and in their publicity.

PUBLICATIONS

Implementation of CCSDS Hyperspectral Image Compression Algorithm on FPGA on board a nanosatellite

Journal name: European Conference on Aeronautics and Space Sciences | Publication date: Jun 30, 2019

- The paper demonstrates an efficient, lowcomplexity, pipelined implementation of the CCSDS algorithm on a Field Programmable Gate Array(FPGA).
- The algorithm was implemented on a Xilinx 7-Series FPGA.
- Algorithm utilizes spectral and spatial redundancy for compression of hyperspectral images.